

Memory FeRAM

4 K (512 × 8) Bit I²C

MB85RC04

■ DESCRIPTION

The MB85RC04 is an FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 512 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC04 is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MB85RC04 has improved to be at least 10¹² cycles, significantly outperforming other nonvolatile memory products in the number.

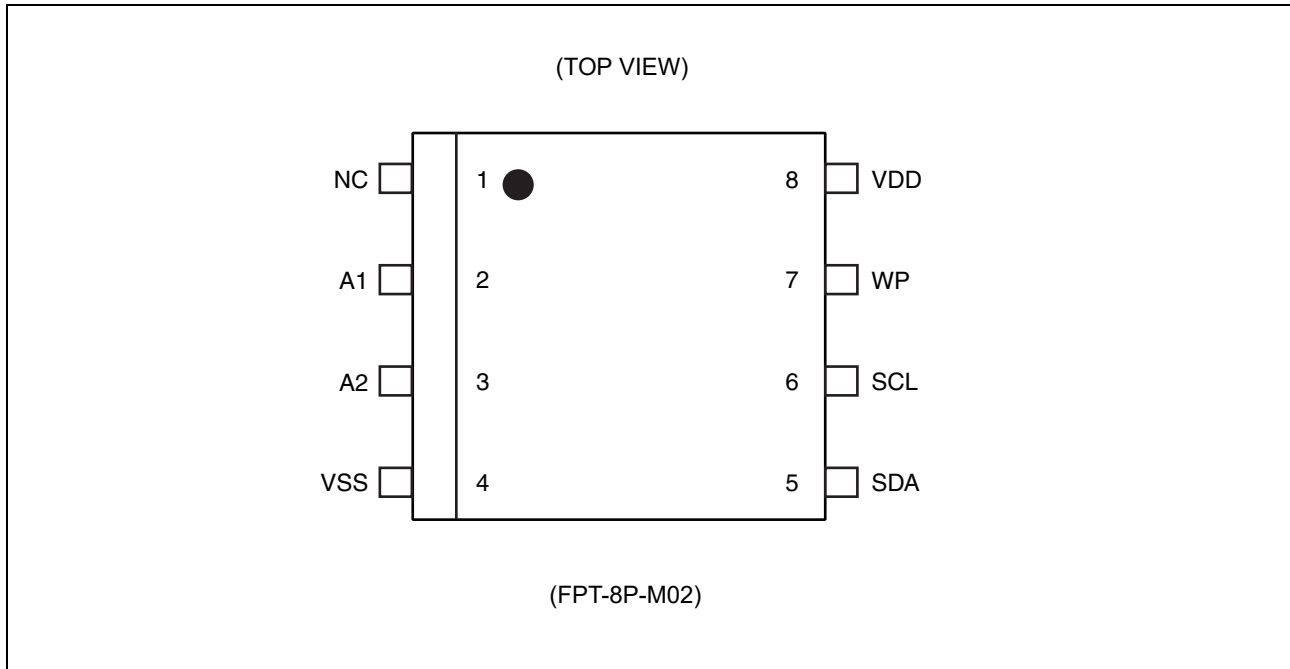
The MB85RC04 does not need a polling sequence after writing to the memory such as the case of Flash memory or E²PROM.

■ FEATURES

- Bit configuration : 512 words × 8 bits
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating frequency : 400 KHz (Max)
- Read/write endurance : 10¹² times / byte
- Data retention : 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
- Operating power supply voltage: 2.7 V to 3.6 V
- Low-power consumption : Operating power supply current 20 μA (Typ @400 KHz)
Standby current 1 μA (Typ)
- Operation ambient temperature range : - 40 °C to + 85 °C
- Package : 8-pin plastic SOP (FPT-8P-M02)
RoHS compliant

MB85RC04

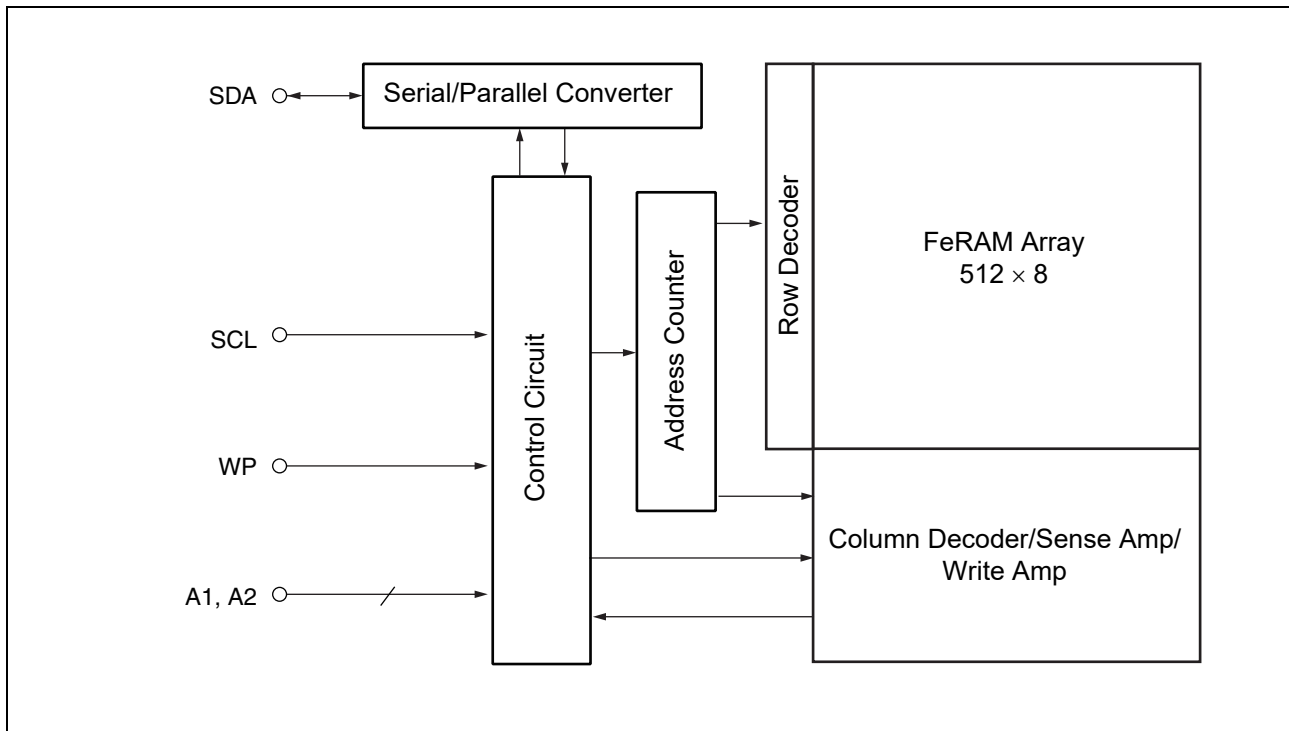
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1	NC	No Connect pin Leave this pin open, or connect to VDD or VSS.
2, 3	A1, A2	Device Address pins The MB85RC04 can be connected to the same data bus up to 4 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A1 and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the "H" level, the writing operation is disabled. When the Write Protect pin is the "L" level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is internally pulled down to VSS pin, and that is recognized as the "L" level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

■ BLOCK DIAGRAM

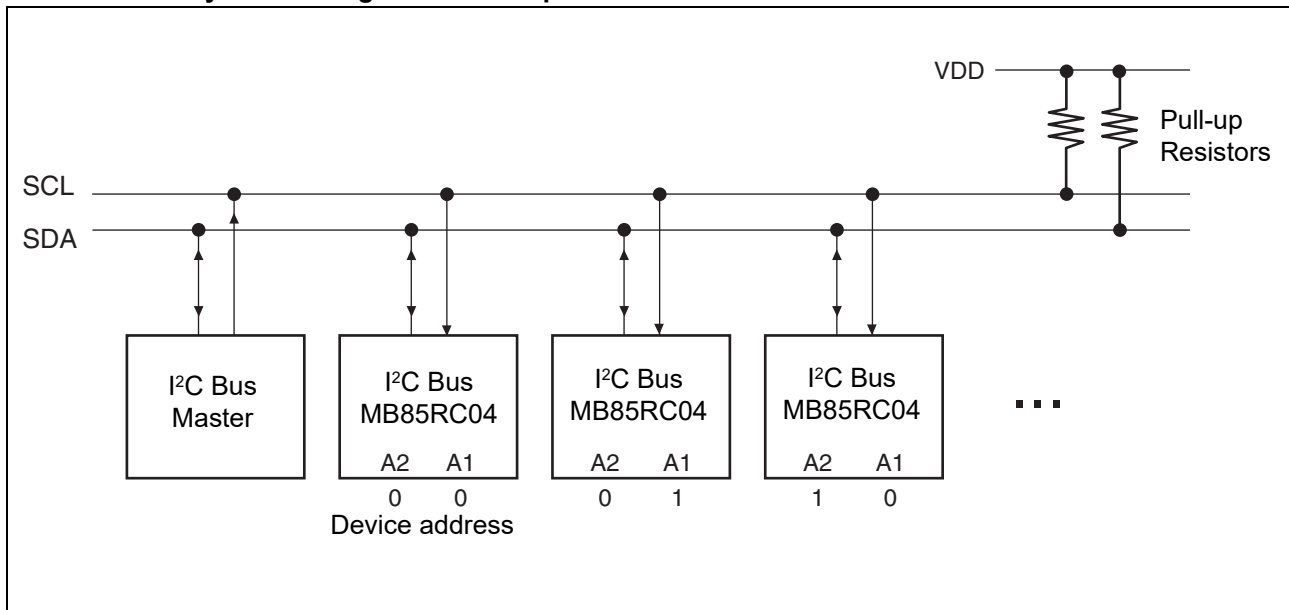


■ I²C (Inter-Integrated Circuit)

The MB85RC04 has the two-wire serial interface; the I²C bus, and operates as a slave device.

The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

● I²C Interface System Configuration Example



■ I²C COMMUNICATION PROTOCOL

The I²C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The SDA signal should change while the SCL is the "L" level. However, as an exception, when starting and stopping communication sequence, the SDA is allowed to change while the SCL is the "H" level.

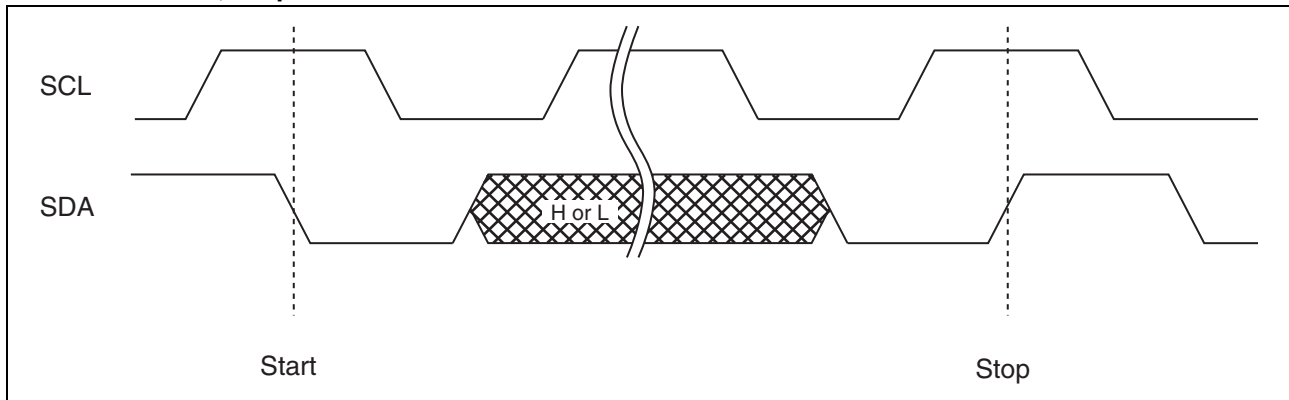
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the "H" level to the "L" level while the SCL input is in the "H" level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the "L" level to the "H" level while the SCL input is in the "H" level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

- Start Condition, Stop Condition



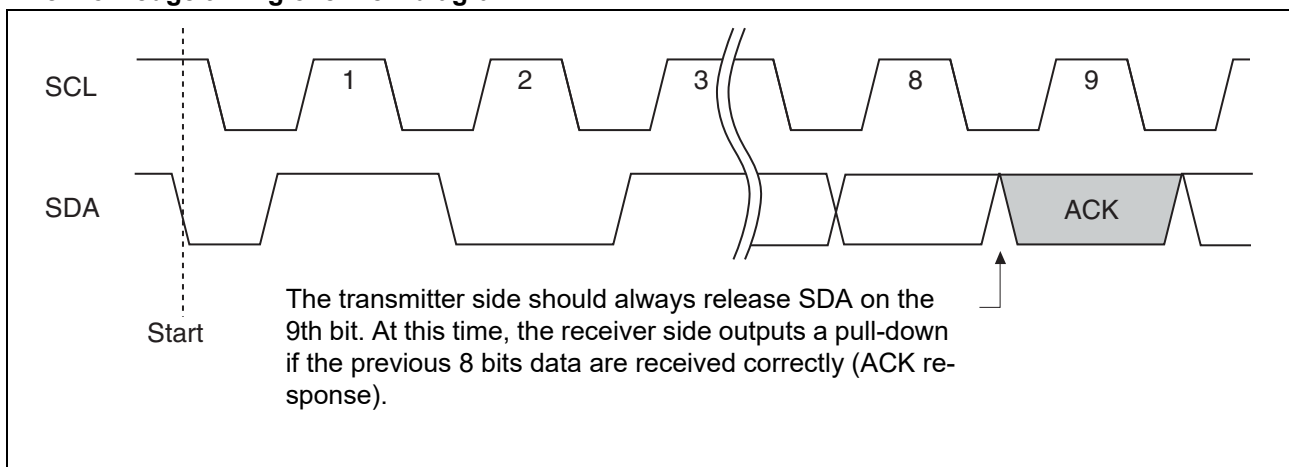
Note : At the write operation, the FeRAM device does not need the programming wait time (t_{wc}) after issuing the Stop Condition.

■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent and received in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the “L” level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK “L” level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK “H” level. The master side generates Stop condition or Start condition in this released bus state.

• Acknowledge timing overview diagram



■ MEMORY ADDRESS STRUCTURE

The MB85RC04 has the memory address buffer to store the 9-bit information for the memory address.

As for byte write, page write and random read commands, the complete 9-bit memory address is configured by inputting the memory upper address (1 bit) and the memory lower address (8 bits), and saved to the memory address buffer. Then access to the memory is performed.

As for a current address read command, the complete 9-bit memory address is configured and saved to the memory address buffer, by inputting the memory upper address (1 bit) and the memory lower address (8 bits) which has saved in the memory address buffer. Then access to the memory is performed.

■ DEVICE ADDRESS WORD

Following the start condition, the 8 bit device address word is input. Inputting the device address word decides whether writing or reading operation. However, the clock is always driven by the master. The device address word (8 bits) consists of a device Type code (4 bits), device address code (2 bits), memory upper address code (1 bit), and a Read/Write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at "1010" for the MB85RC04.

- Device Address Code (2 bits): A1, A2

Following the device type code, the 2 bits of the device address code are input in order of A2 and A1.

The device address code identifies one device from up to 4 devices connected to the bus.

Each MB85RC04 is given a unique 2 bits code on the device address pin (external hardware pin A2 and A1). The slave only responds if the received device address code is equal to this unique 2 bits code.

- Memory Upper Address Code (1 bit): A8

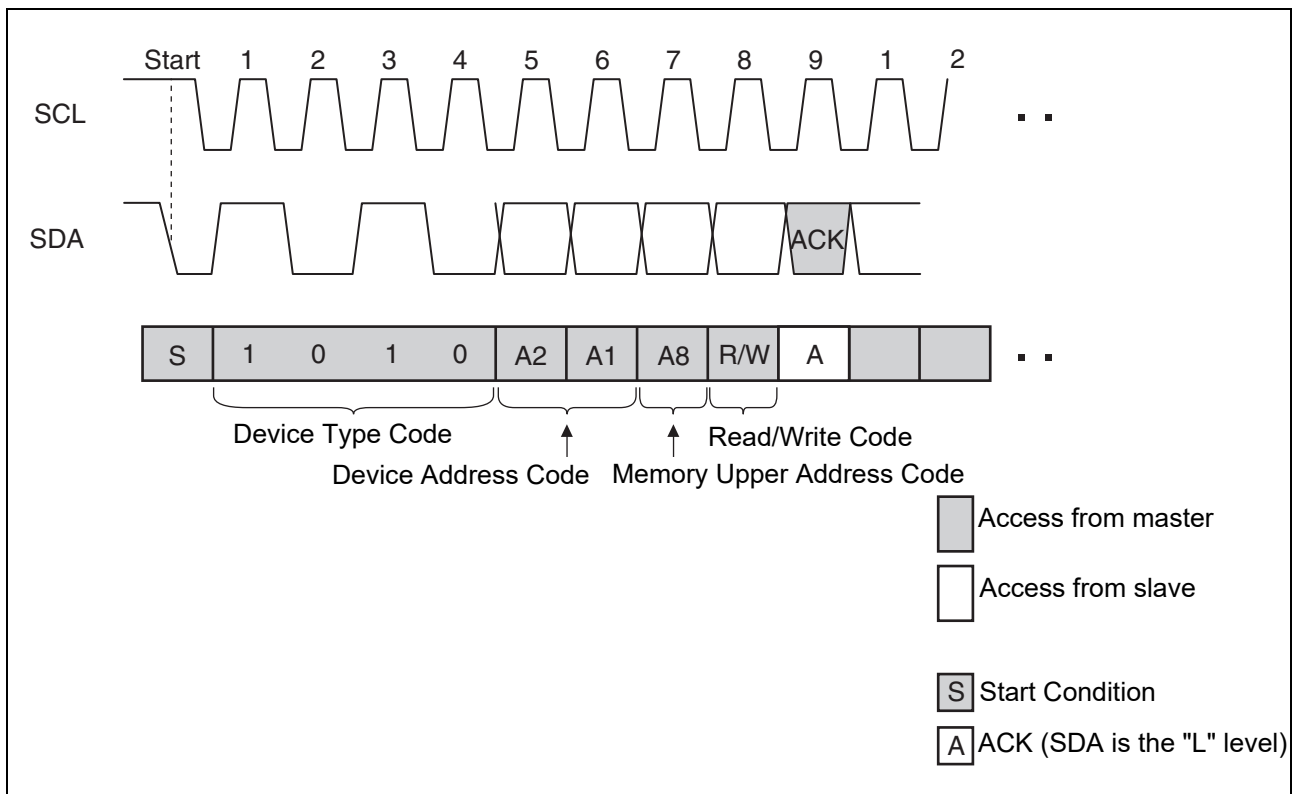
Following the device address code, the 1-bit memory upper address code are input.

This bit is not the setting bit for the slave address, but the upper 1-bit setting bit for the memory address.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (Read/Write) code. When the R/W code is "0" input, a write operation is enabled, and the R/W code is "1" input, a read operation is enabled for the MB85RC04. If the device type code is not "1010" or the device address code is not equal to the setting of the external device address pins, the Read/Write operation is not performed and the standby state is chosen.

• Device Address Word



■ DATA STRUCTURE

The master inputs the device address word (8 bits) following the start condition, and then the slave outputs the Acknowledge “L” level on the 9th bit. After confirming the Acknowledge response, the sequential 8-bit memory lower address is input, to the byte write, page write and random read commands.

As for the current address read command, inputting the memory lower address is not performed, and the address buffer lower 8-bit is used as the memory lower address.

When inputting the memory lower address is finished, the slave outputs the Acknowledge “L” level on the 9th bit again.

Afterwards, the input and the output data continue in 8-bit units, and then the Acknowledge “L” level is output for every 8-bit data.

■ FeRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC04 performs the high speed write operations, so any waiting time for an ACK* by the acknowledge polling does not occur.

- *: In E²PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

The entire memory array can be write protected by setting the WP pin to the “H” level. When the WP pin is set to the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

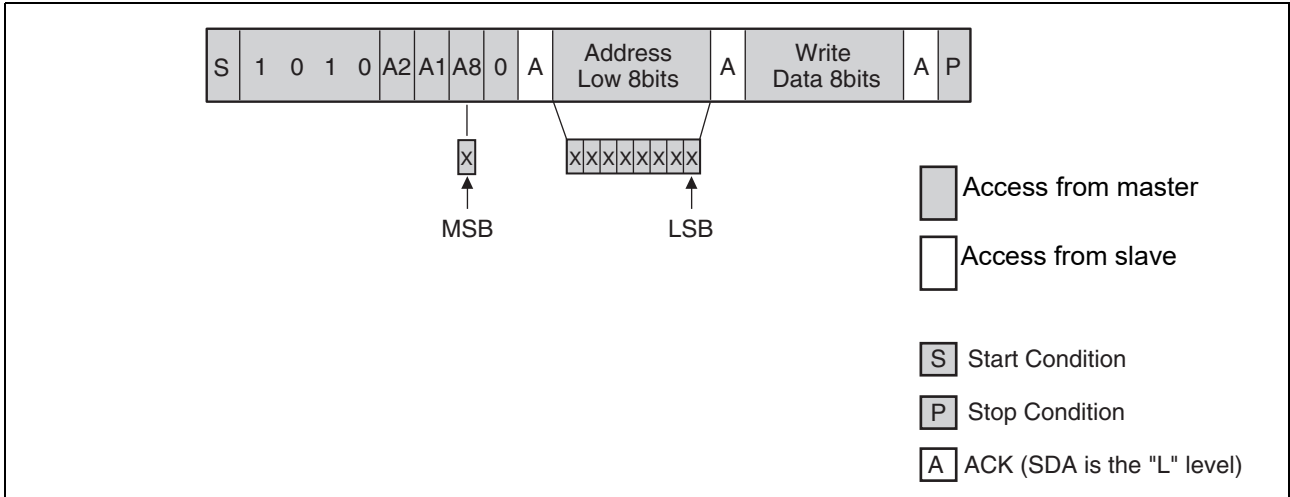
Do not change the WP signal level during the communication period from the start condition to the stop condition.

Note : The WP pin is pulled down internally to the VSS pin, therefore if the WP pin is open, the pin status is recognized as the “L” level (write enabled).

■ COMMAND

• Byte Write

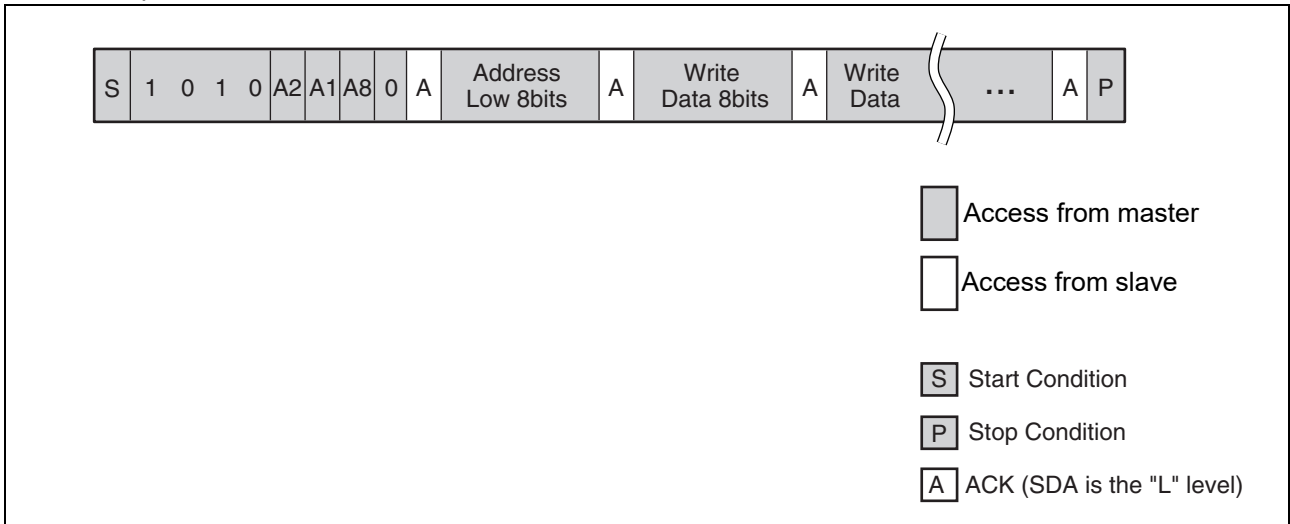
If the device address word (R/W "0" input) is sent after the start condition, the slave responds with an ACK. After this ACK, write memory addresses and write data are sent in the same way, and the write ends by generating a stop condition at the end.



• Page Write

If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (000H) at the end of the address. Therefore, if more than 512bytes are sent, the data is overwritten in order starting from the start of the memory address that was written first.

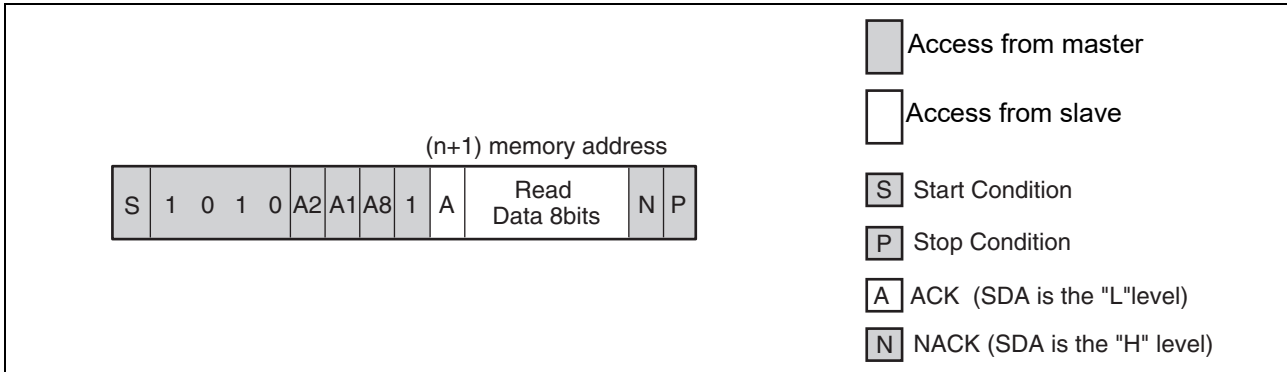
As the FeRAM performs the high-speed write operations, the data will be written to FeRAM right after the ACK response finished.



• Current Address Read

If the last write or read operation finishes successfully up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 9 bits).

When sending this command without turning the power off, it is possible to read from the memory address $n+1$ which adds 1 to the total 9-bit memory address n , which consists of the 1-bit memory upper address from the device address word input and the lower 8-bit of the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address (000_H). The current address (address that the memory address buffer indicates) is undefined immediately after turning the power on.

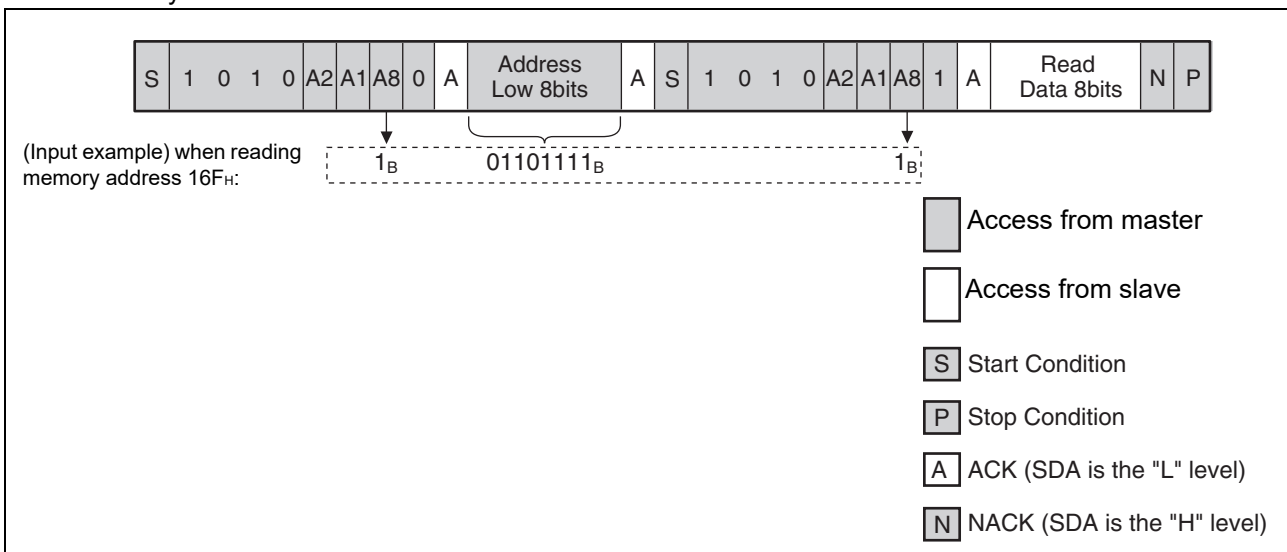


• Random Read

The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W "1" input).

Setting values for the first and the second memory upper address codes should be the same (an example is shown in below).

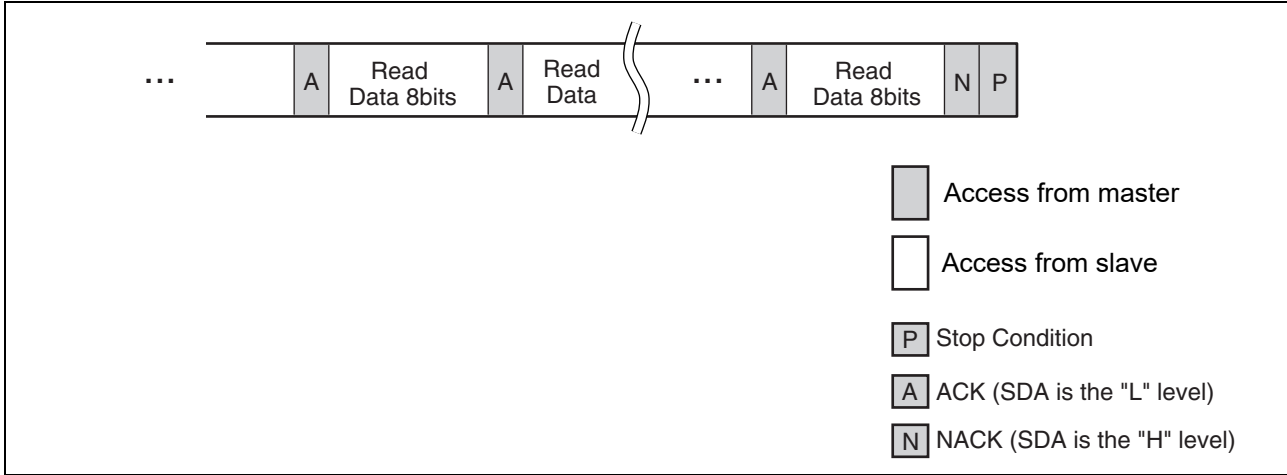
The final NACK (SDA is the "H" level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



MB85RC04

- Sequential Read

Data can be received continuously following the Device address word (R/W "1" input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the read address automatically rolls over to the first memory address (000H) and keeps reading.

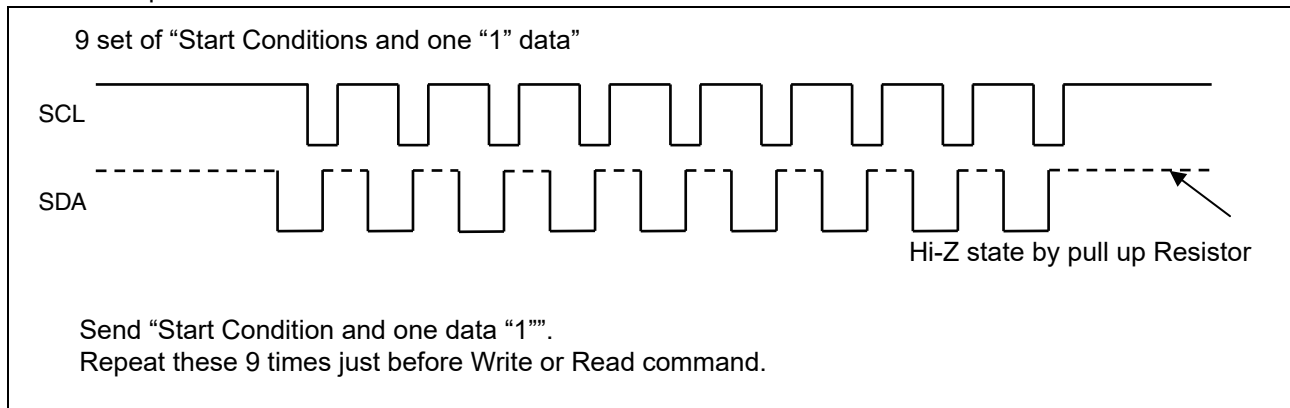


■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I²C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

(1) Software Reset Sequence

Since the slave side may be outputting "L" level, do not force to drive "H" level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.



(2) Command Retry

Command retry is useful to recover from failure response during I²C communication.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	- 0.5	+4.0	V
Input voltage*	V_{IN}	- 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Output voltage*	V_{OUT}	- 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Operation ambient temperature	T_A	- 40	+ 85	°C
Storage temperature	T_{stg}	- 55	+ 125	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage ^{*1}	V_{DD}	2.7	—	3.6	V
Operation ambient temperature ^{*2}	T_A	- 40	—	+ 85	°C

*1: These parameters are based on the condition that VSS is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	I _{LI}	V _{IN} = 0 V to V _{DD}	—	—	1	μA
Output leakage current*2	I _{LO}	V _{OUT} = 0 V to V _{DD}	—	—	1	μA
Operating power supply current	I _{DD}	SCL = 400 kHz	—	20	40	μA
Standby current	I _{SB}	SCL, SDA = V _{DD} WP = 0 V or V _{DD} or Open Under Stop Condition T _A = +25 °C	—	1	5	μA
“H” level input voltage	V _{IH}	V _{DD} = 2.7 V to 3.6 V	V _{DD} × 0.8	—	V _{DD} + 0.5 (≤ 4.0)	V
“L” level input voltage	V _{IL}	V _{DD} = 2.7 V to 3.6 V	− 0.5	—	V _{DD} × 0.2	V
“L” level output voltage	V _{OL}	I _{OL} = 3 mA	—	—	0.4	V
Input resistance for WP, A1, and A2 pins	R _{IN}	V _{IN} = V _{IL} (Max)	50	—	—	kΩ
		V _{IN} = V _{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

2. AC Characteristics

Parameter	Symbol	Value				Unit
		STANDARD MODE		FAST MODE		
		Min	Max	Min	Max	
SCL clock frequency	F _{SCL}	0	100	0	400	kHz
Clock high time	T _{HIGH}	4000	—	600	—	ns
Clock low time	T _{LOW}	4700	—	1300	—	ns
SCL/SDA rising time	T _r	—	1000	—	300	ns
SCL/SDA falling time	T _f	—	300	—	300	ns
Start condition hold	T _{HD:STA}	4000	—	600	—	ns
Start condition setup	T _{SU:STA}	4700	—	600	—	ns
SDA input hold	T _{HD:DAT}	0	—	0	—	ns
SDA input setup	T _{SU:DAT}	250	—	100	—	ns
SDA output hold	T _{DH:DAT}	0	—	0	—	ns
Stop condition setup	T _{SU:STO}	4000	—	600	—	ns
SDA output access after SCL falling	T _{AA}	—	3000	—	900	ns
Pre-charge time	T _{BUF}	4700	—	1300	—	ns
Noise suppression time (SCL and SDA)	T _{SP}	—	50	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : STANDARD MODE and FAST MODE 2.7 V to 3.6 V

Operation ambient temperature : - 40 °C to + 85 °C

Input voltage magnitude : $V_{DD} \times 0.2$ to $V_{DD} \times 0.8$

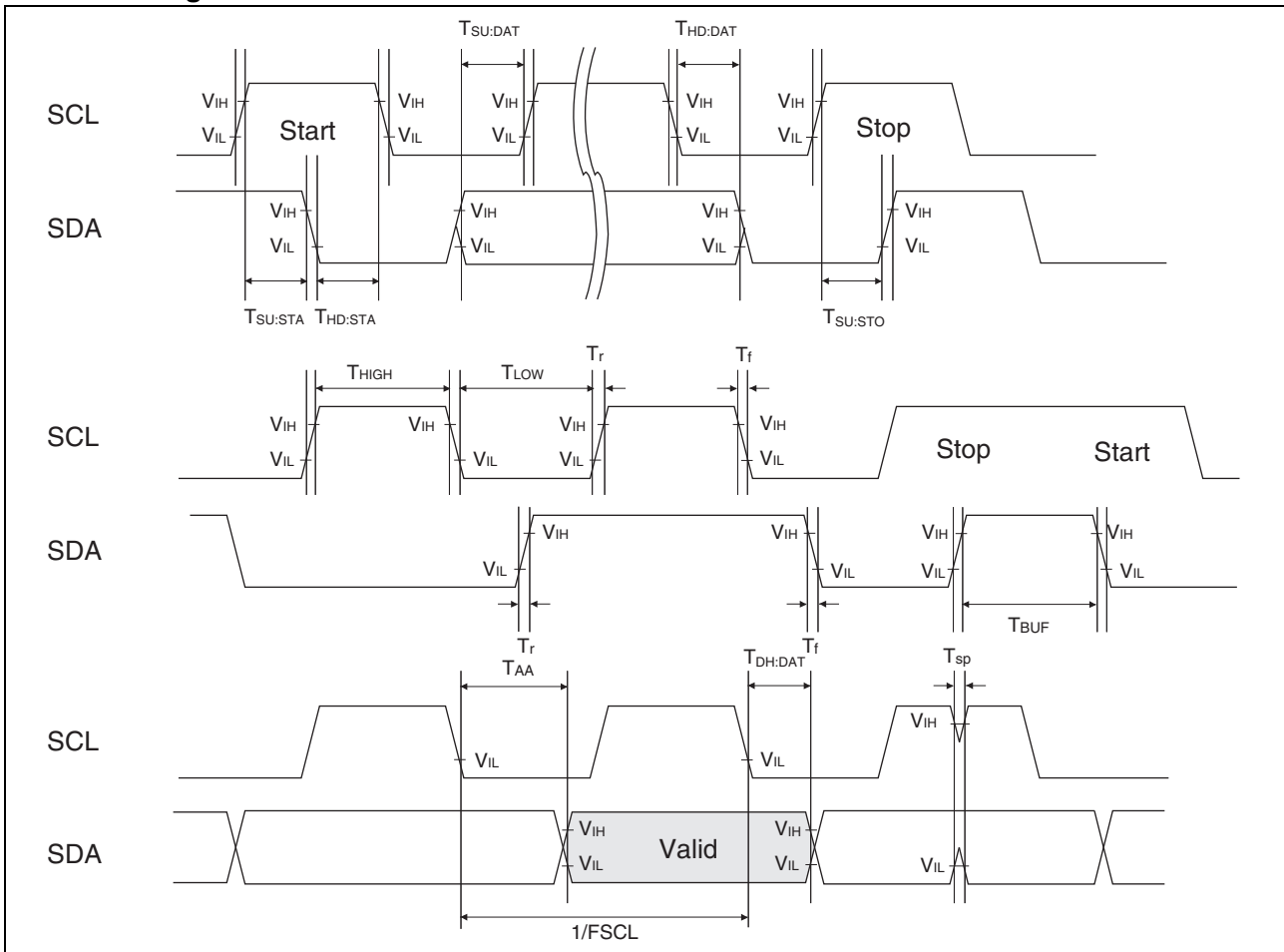
Input rising time : 5 ns

Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

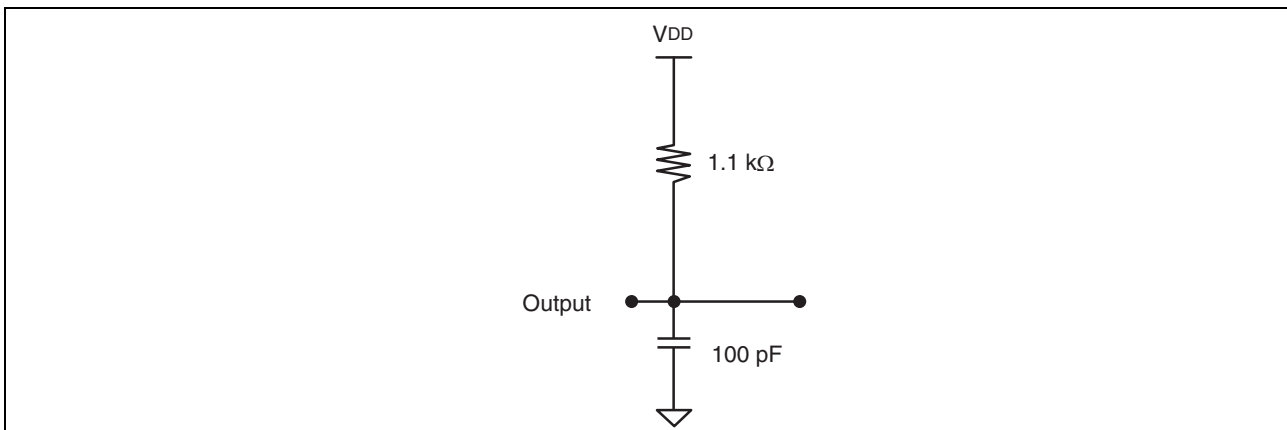
3. AC Timing Definitions



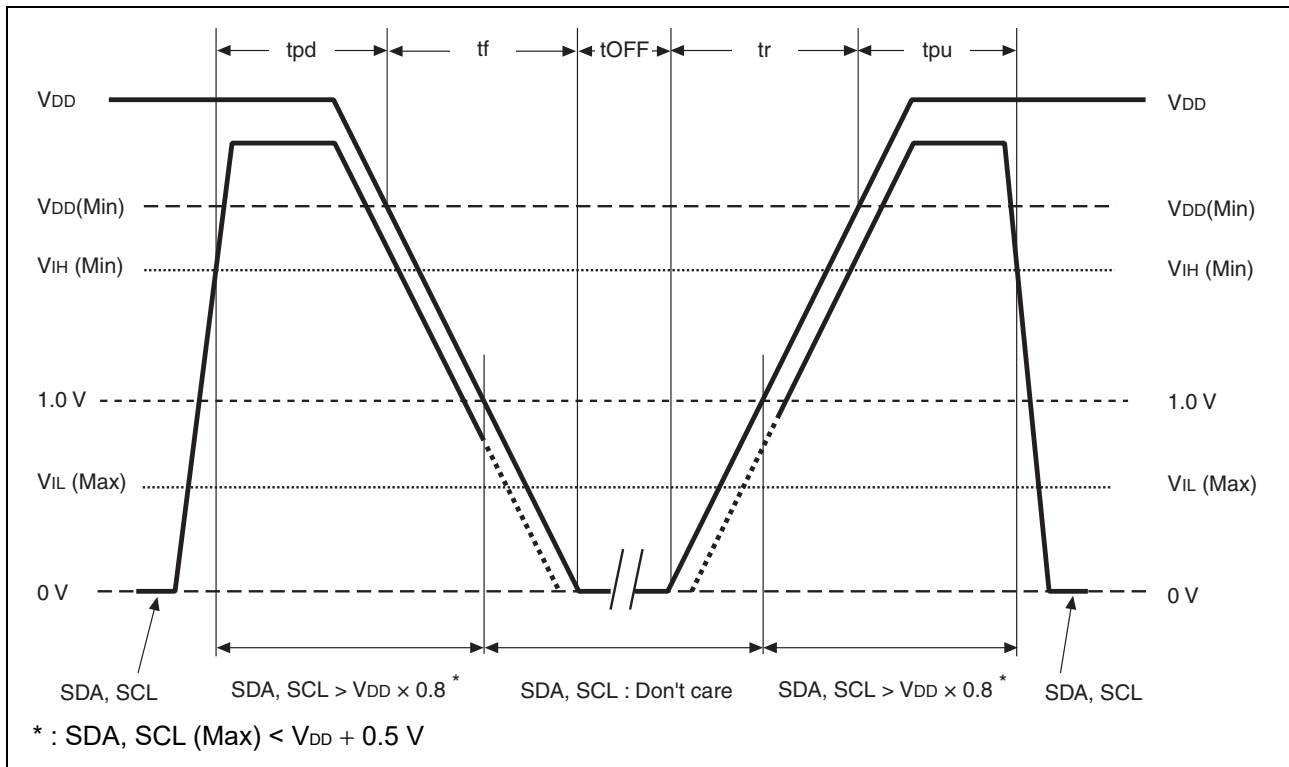
4. Pin Capacitance

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	$V_{DD} = V_{IN} = V_{OUT} = 0\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ }^\circ\text{C}$	—	—	15	pF
Input capacitance	C_{IN}		—	—	15	pF

5. AC Test Load Circuit



■ POWER ON SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	85	—	ns
Power supply rising time	tr	0.01	—	ms
Power supply falling time	tf	0.01	—	ms
Power off time	tOFF	50	—	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10 ¹²	—	Times/byte	Operation Ambient Temperature T _A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T _A = + 85 °C
	95	—		Operation Ambient Temperature T _A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T _A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

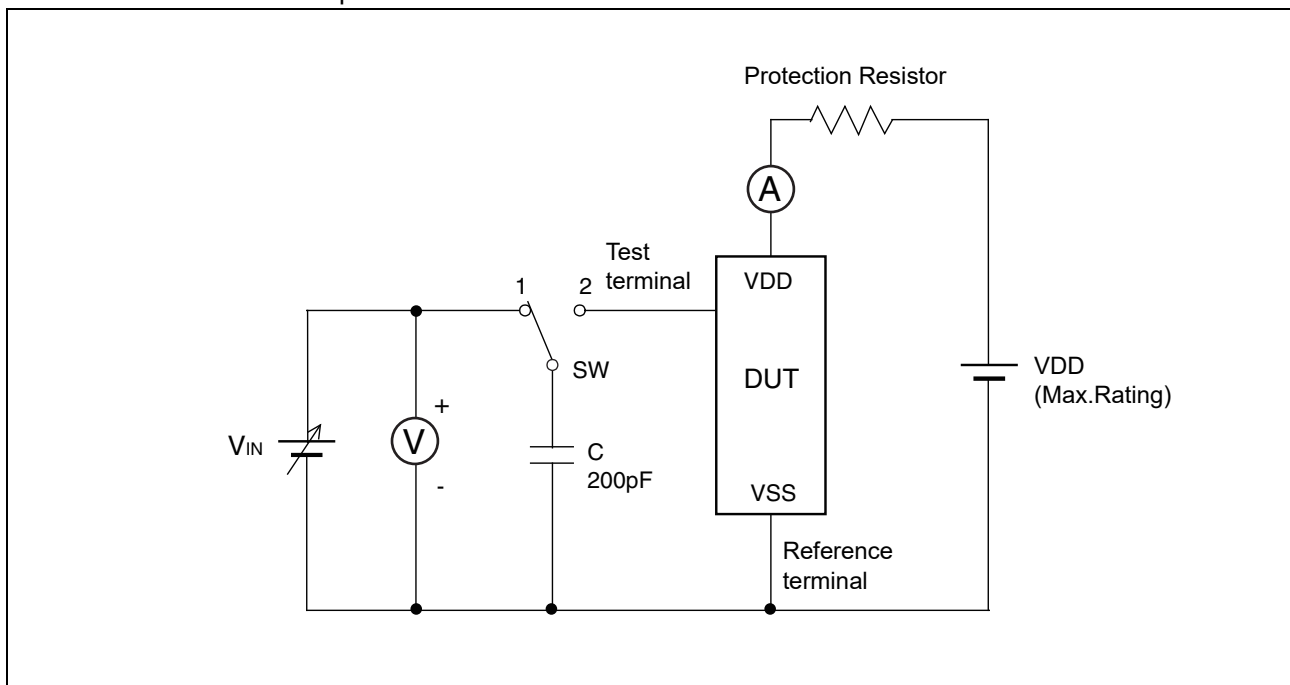
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.
- During the access period from the start condition to the stop condition, keep the level of WP, A1, and A2 pins to the “H” level or the “L” level.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RC04PNF-G-JNE1	$\geq 2000 \text{ V} $
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

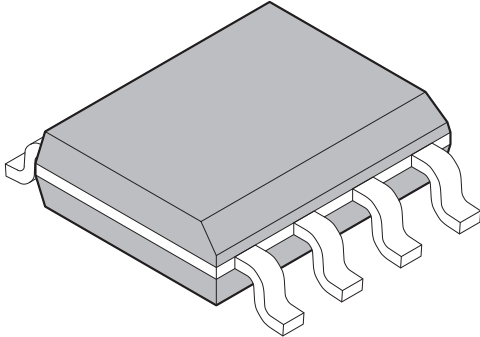
MB85RC04

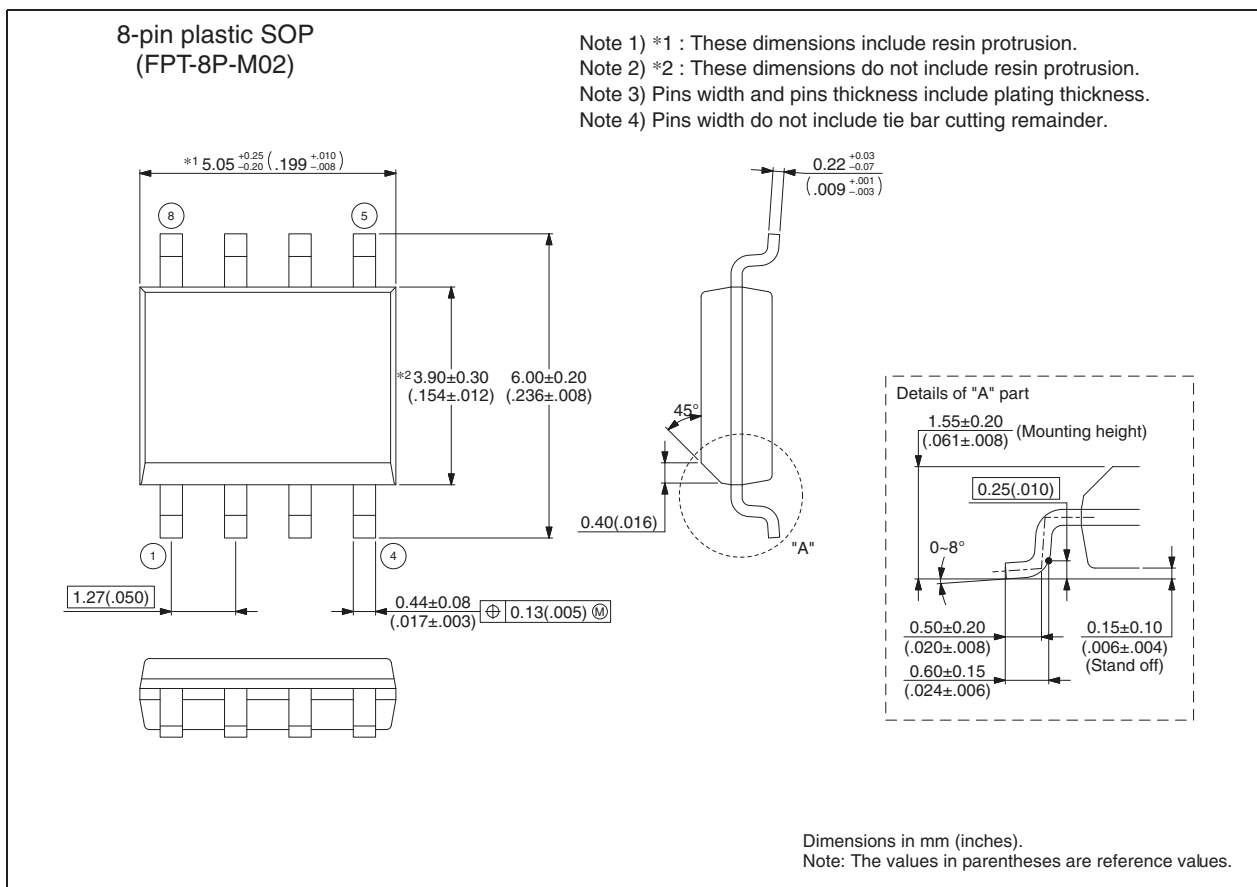
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RC04PNF-G-JNE1	8-pin, plastic SOP (FPT-8P-M02)	Tube	—*
MB85RC04PNF-G-JNERE1	8-pin, plastic SOP (FPT-8P-M02)	Embossed Carrier tape	1500

*: Please contact our sales office about minimum shipping quantity.

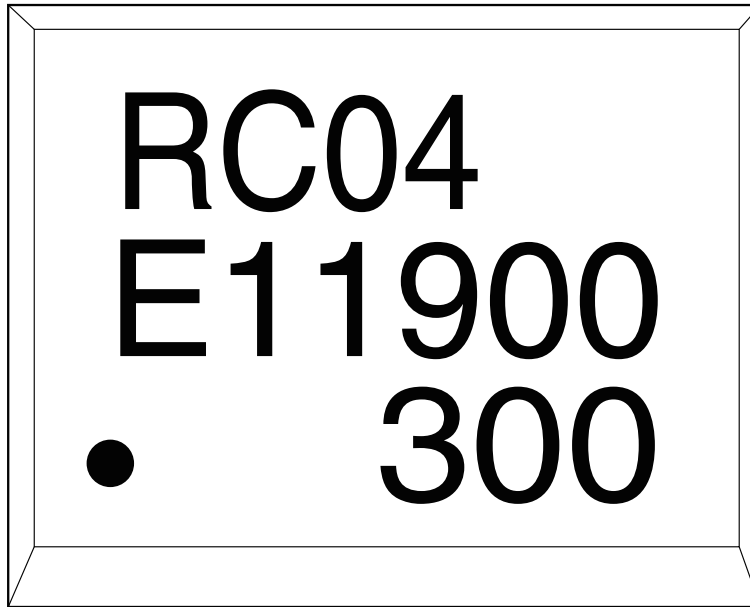
■ PACKAGE DIMENSION

<p>8-pin plastic SOP</p>  <p>(FPT-8P-M02)</p>	Lead pitch	1.27 mm	
	Package width × package length	3.9 mm × 5.05 mm	
	Lead shape	Gullwing	
	Sealing method	Plastic mold	
	Mounting height	1.75 mm MAX	



■ MARKING

[MB85RC04PNF-G-JNE1]
[MB85RC04PNF-G-JNERE1]



[FPT-8P-M02]

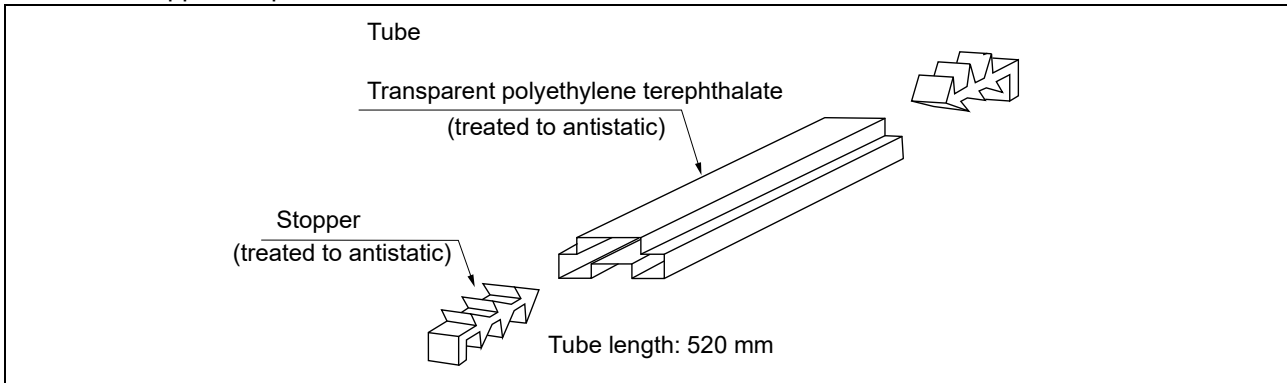
RC04: Product name
E11900: E1(Environment code) + 1900(Year and Week code)
300: 3(Factory code) + 00(Trace code)

■ PACKING INFORMATION

1. Tube

1.1 Tube Dimensions

- Tube/stopper shape



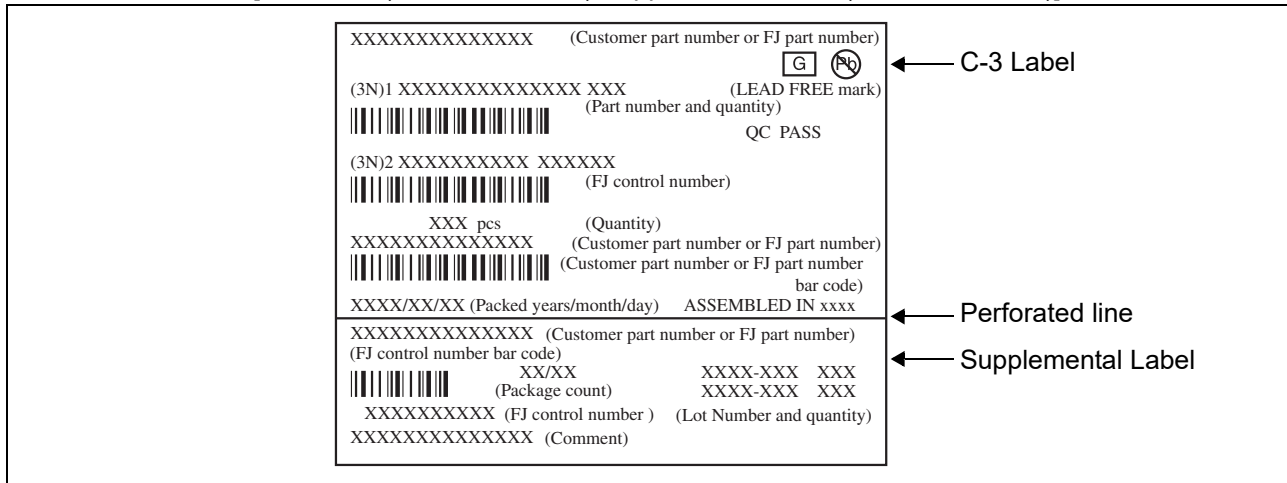
Tube cross-sections and Maximum quantity

Package form	Package code	Maximum quantity		
		pcs/ tube	pcs/inner box	pcs/outer box
SOP, 8, plastic (2)	FPT-8P-M02	95	7600	30400
<p>Transparent polyethylene terephthalate</p>				

(Dimensions in mm)

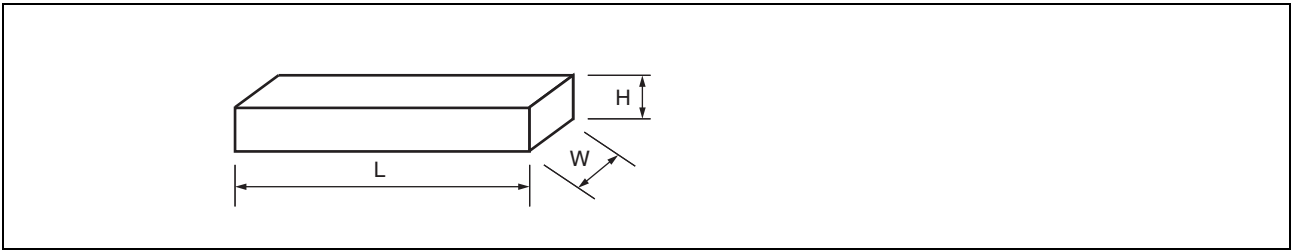
1.2 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.3 Dimensions for Containers

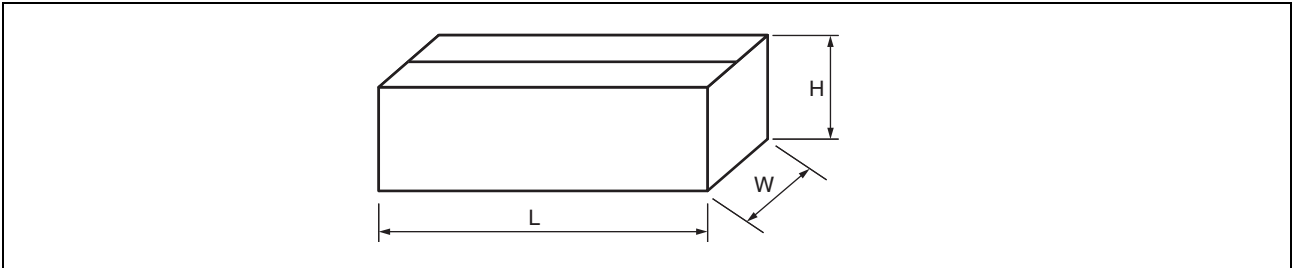
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
549	277	180

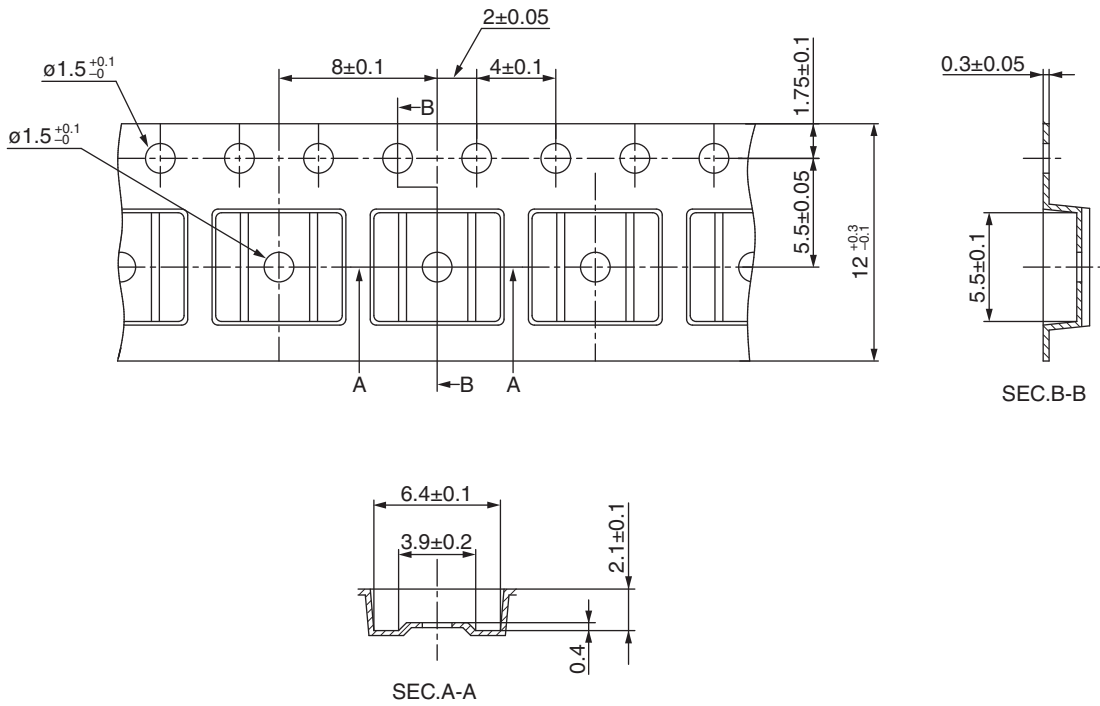
(Dimensions in mm)

MB85RC04

2. Emboss Tape

2.1 Tape Dimensions

PKG code	Maximum storage capacity		
	pcs/reel	pcs/inner box	pcs/outer box
FPT-8P-M02	1500	1500	10500



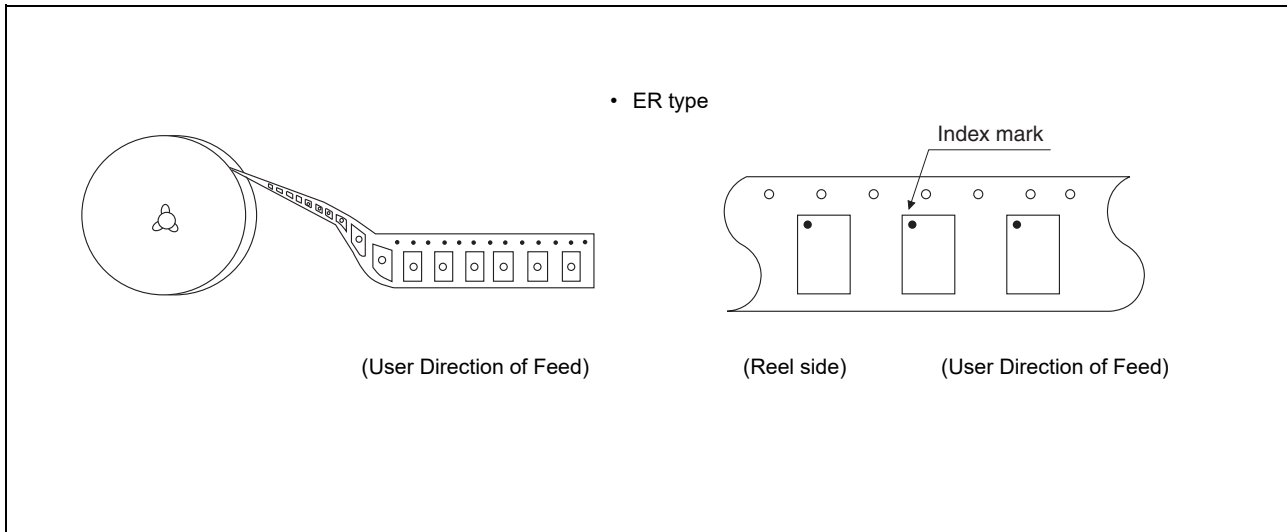
(Dimensions in mm)

Material : Conductive polystyrene

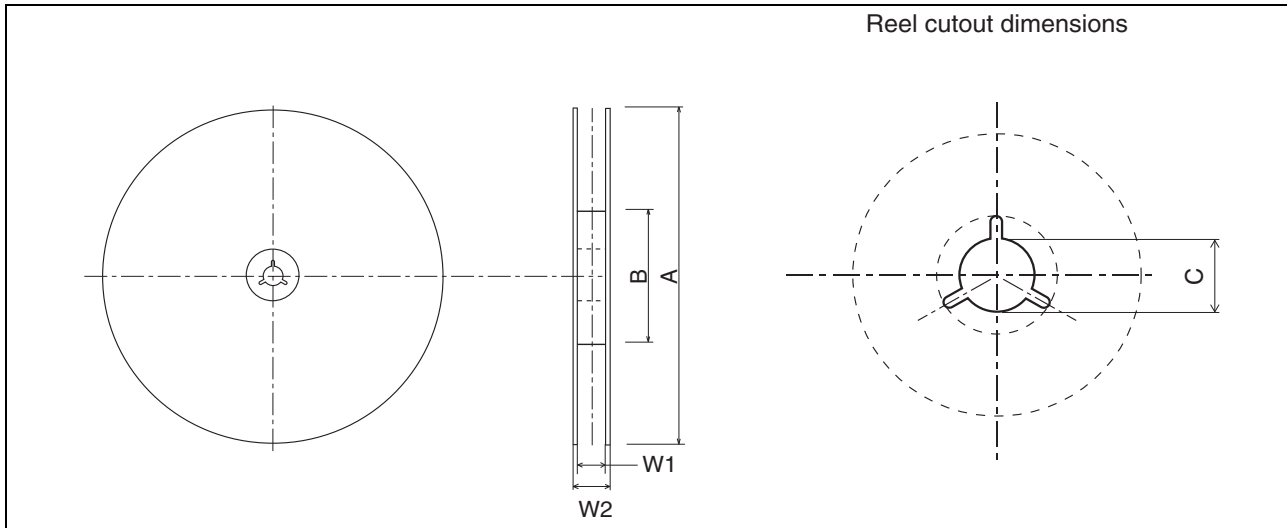
Heat proof temperature : No heat resistance.

Package should not be baked by using tape and reel.

2.2 IC orientation



2.3 Reel dimensions

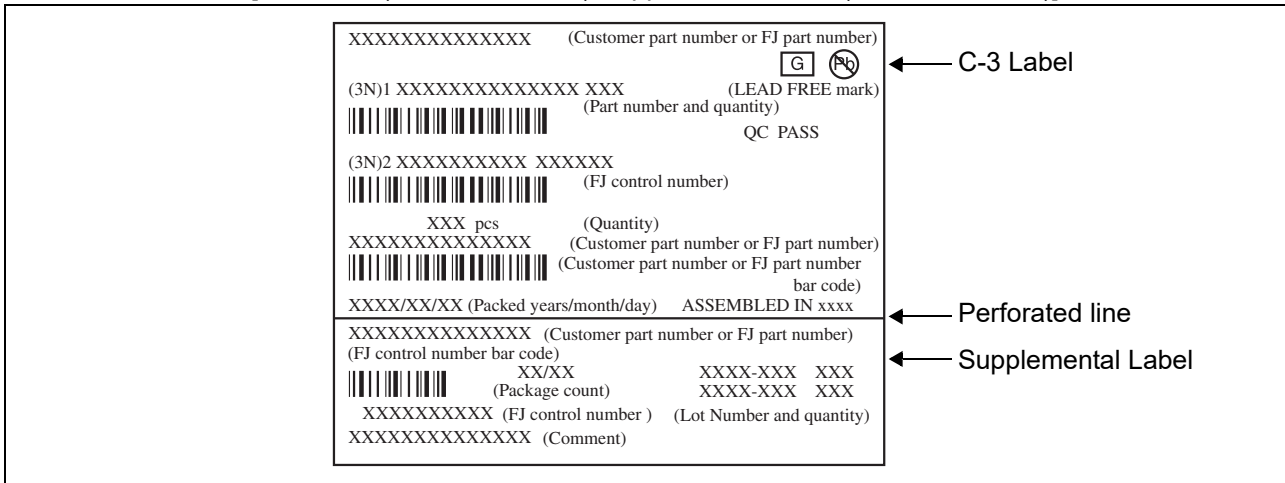


Dimensions in mm

Tape width	A	B	C	W1	W2
12	330	100	13	13.7	17.5

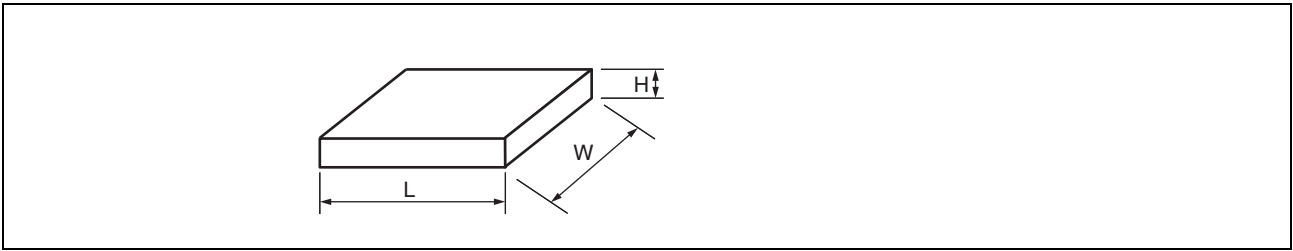
2.4 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



2.5 Dimensions for Containers

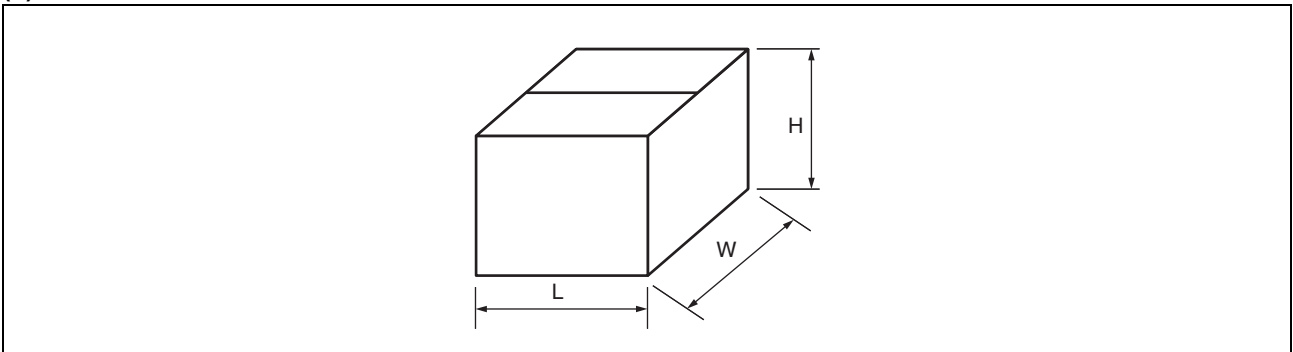
(1) Dimensions for inner box



Tape width	L	W	H
12	365	345	40

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
415	400	315

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
—	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM

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Edited: Sales and Marketing Division